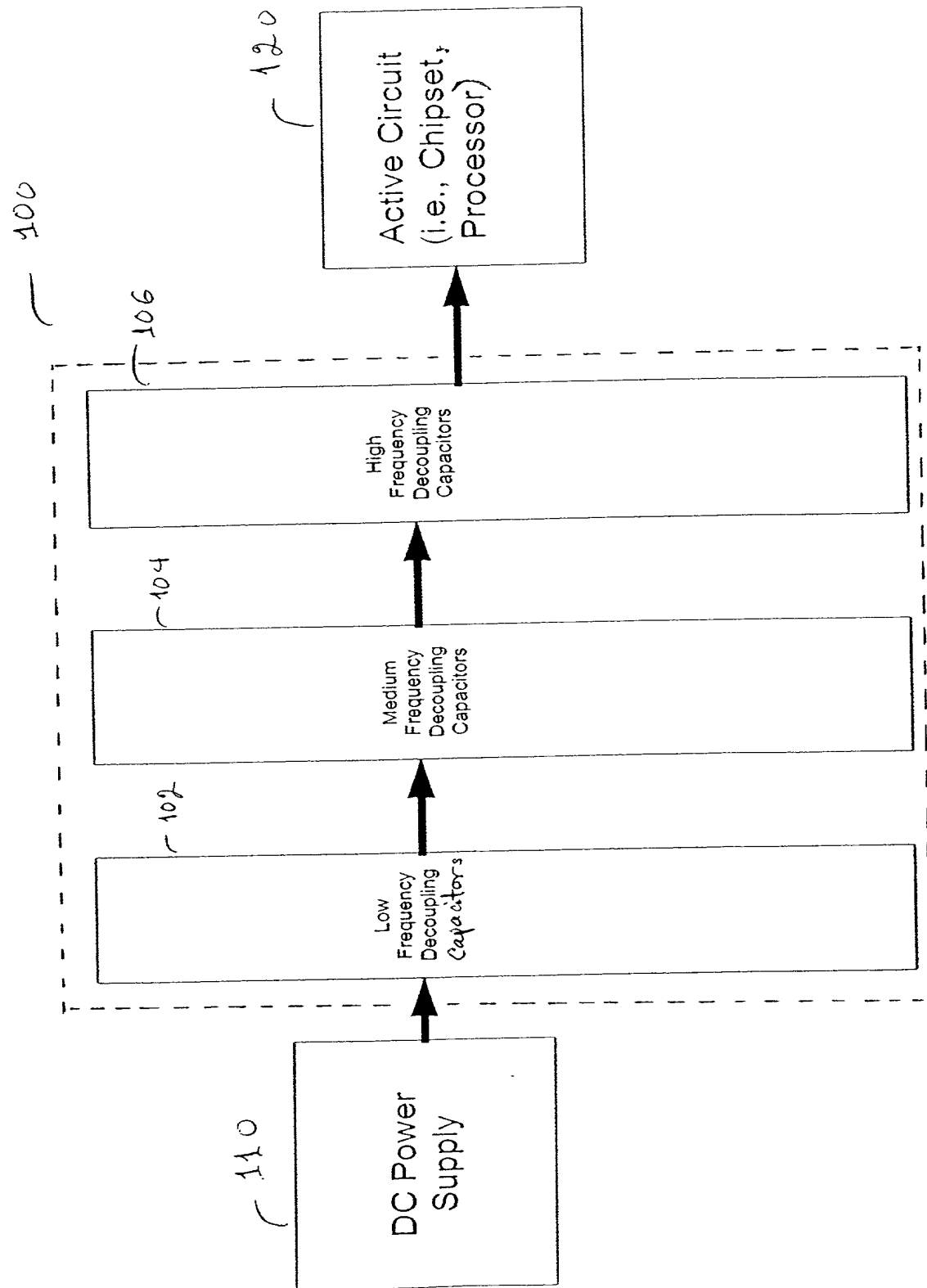


FIG. 1 basic power delivery system



I/O Cell #1

I/O Cell #2

I/O Cell #3

I/O Cell #4

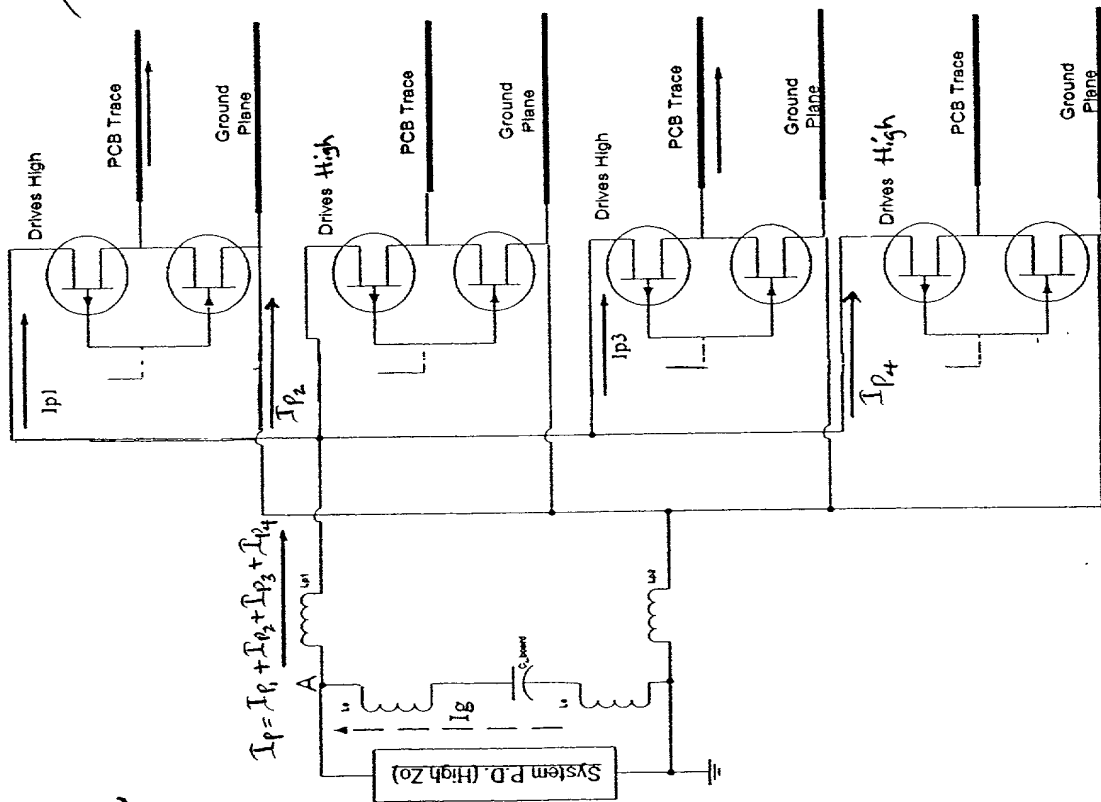


FIG. 2

2/0 cell #1

2/0 cell #2

2/0 cell #3

2/0 cell #4

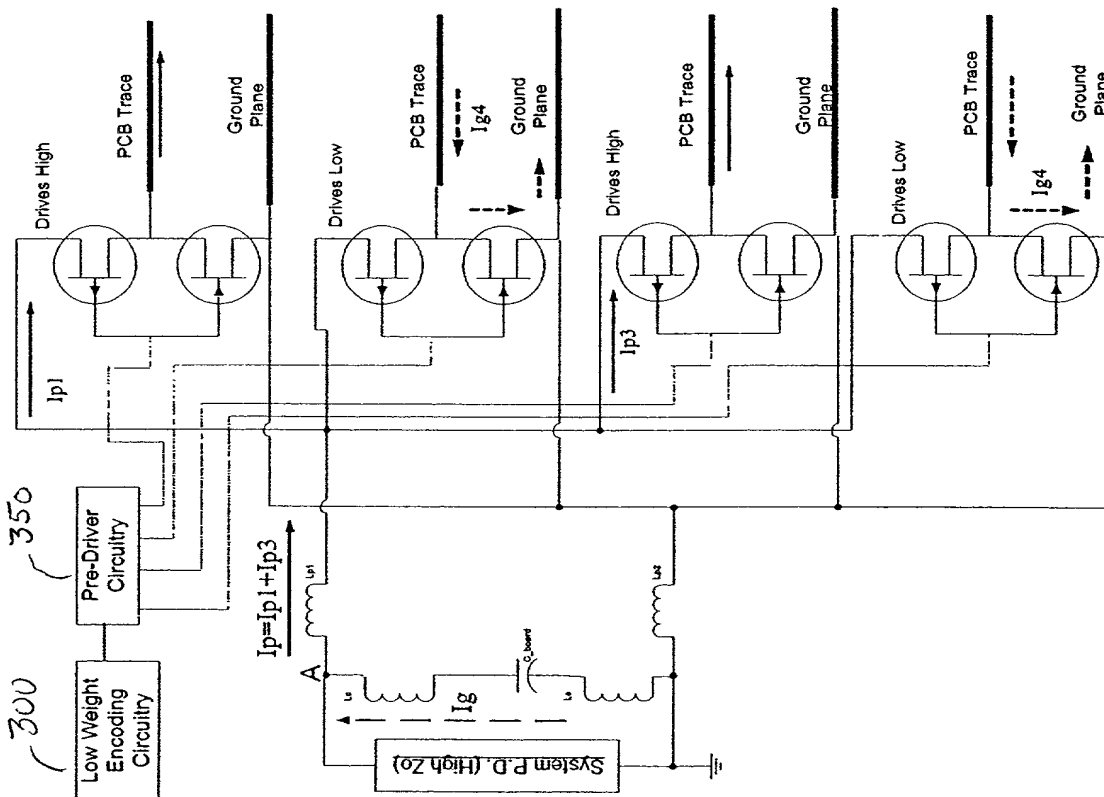


FIG. 3

100

FIG. 4

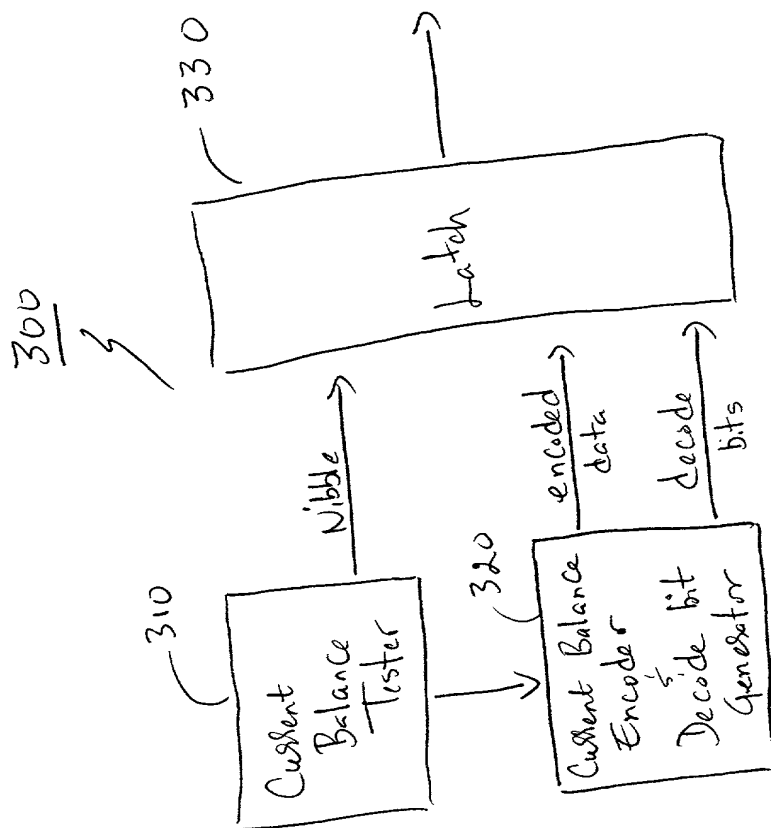


FIG. 5

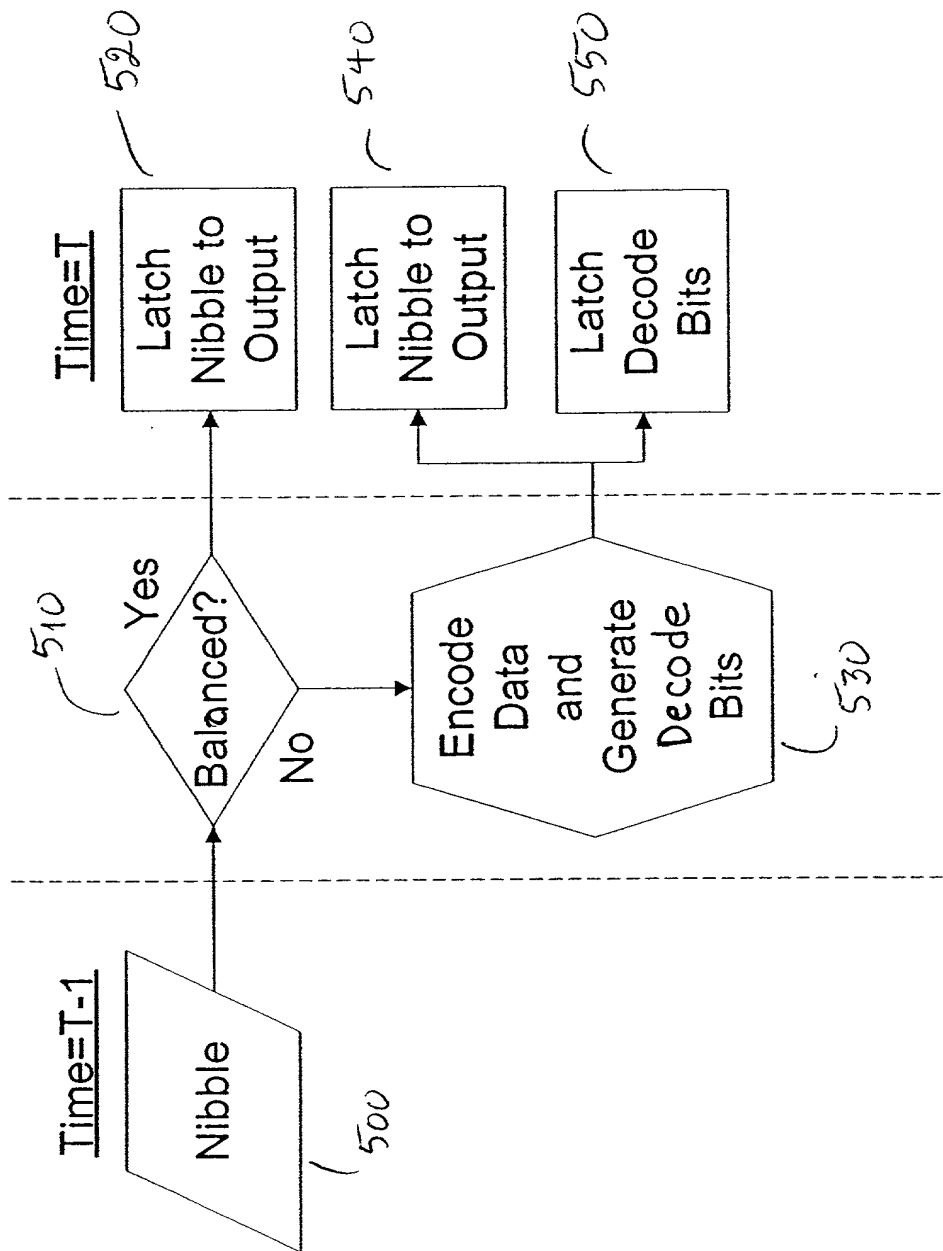


FIG. 6A

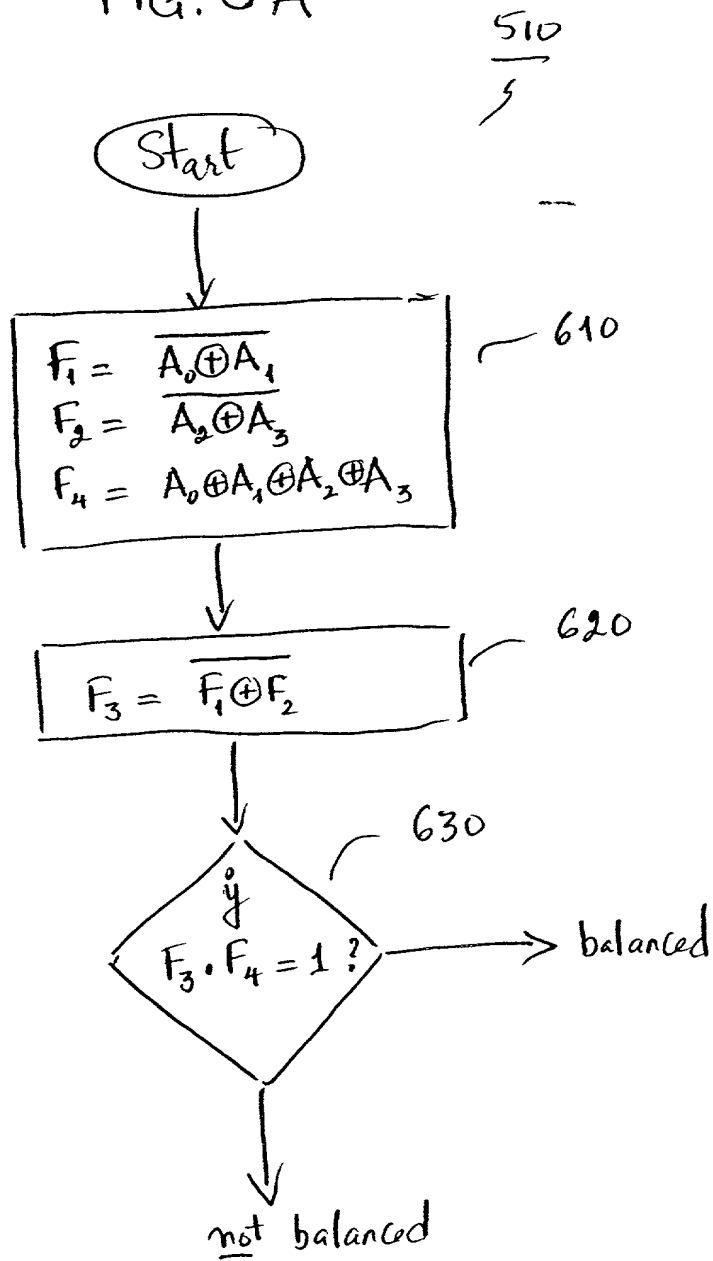


FIG. 7A

530



start

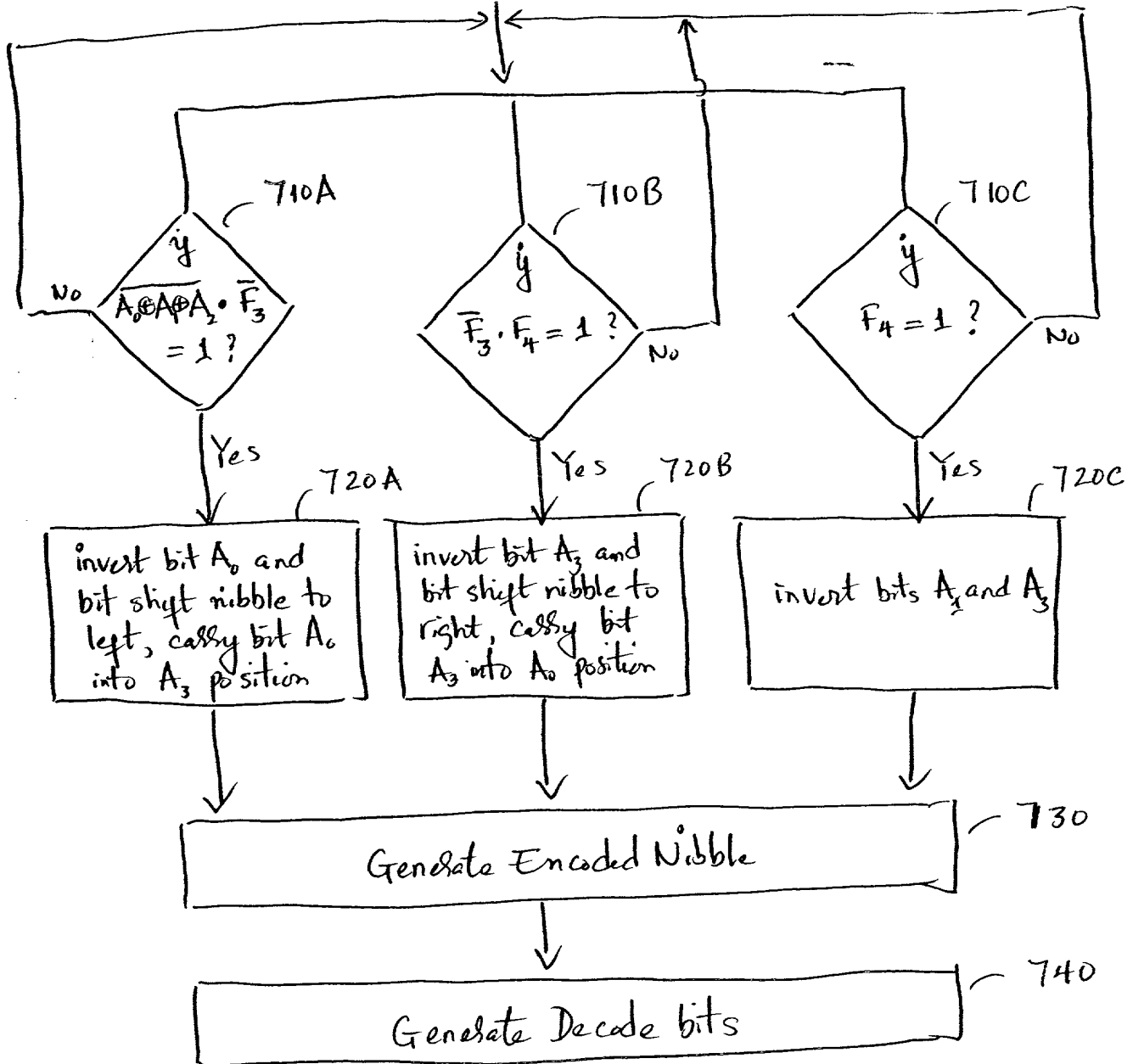


FIG. 6B - TABLE #1

A_0	A_1	A_2	A_3	F_1	F_2	F_3	F_4	$F_3 \bullet F_4$
0	0	0	0	1	1	1	0	0
0	0	0	1	1	0	0	1	0
0	0	1	0	1	0	0	1	0
0	0	1	1	1	1	1	1	1
0	1	0	0	1	0	0	1	0
0	1	0	1	0	0	1	1	1
0	1	1	0	0	1	0	1	0
0	1	1	1	0	0	1	1	1
1	0	0	0	0	1	0	1	0
1	0	0	1	0	1	0	1	0
1	0	1	0	0	0	1	1	0
1	0	1	1	0	0	1	1	0
1	1	0	0	0	1	0	1	0
1	1	0	1	0	1	0	1	0
1	1	1	0	0	0	1	1	0
1	1	1	1	0	0	1	1	0
1	1	1	1	1	1	1	1	1

FIG. 7B - TABLE #2

Encoded Nibble				Decode Bits			
A_0	A_1	A_2	A_3	A_0	A_1	A_2	A_3
0	0	0	0	0	1	0	1
0	0	0	1	0	0	1	1
0	0	1	0	1	0	0	1
0	0	1	1	1	0	1	0
0	1	0	0	0	0	1	0
0	1	0	1	0	0	0	1
1	0	0	0	0	1	1	0
1	0	0	1	1	1	0	0
1	0	1	0	0	1	0	1
1	0	1	1	0	0	0	1
1	1	0	0	0	1	1	0
1	1	0	1	1	1	0	0
1	1	1	0	1	0	1	0
1	1	1	1	1	0	0	1
1	1	1	1	1	0	1	1